HOMEWORK 6

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**Description of your circuit:**

(Please describe the function and dataflow of the circuit.)

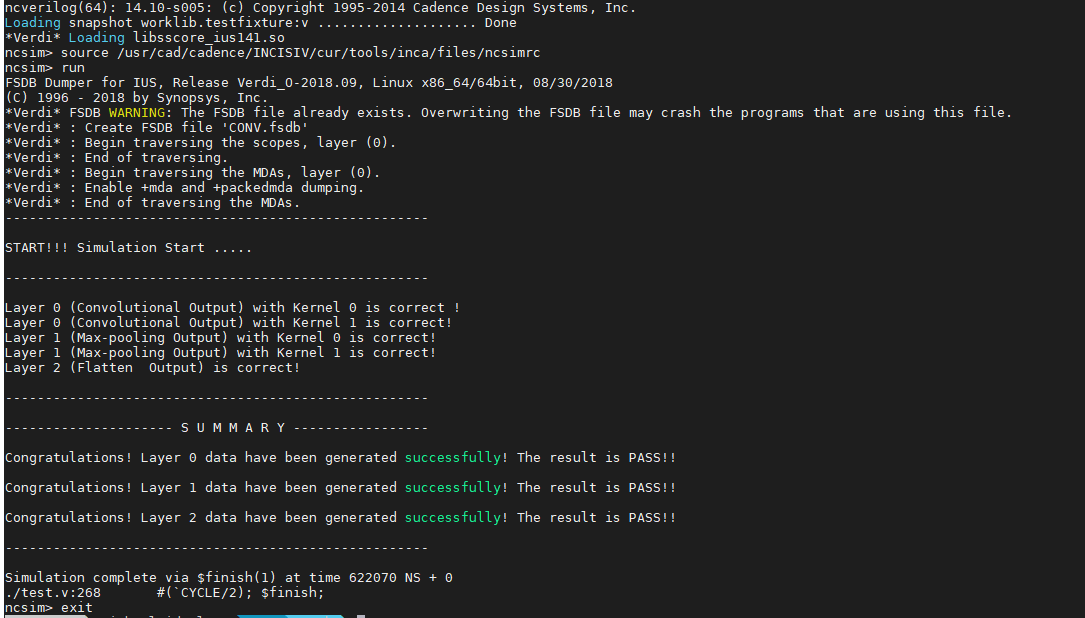
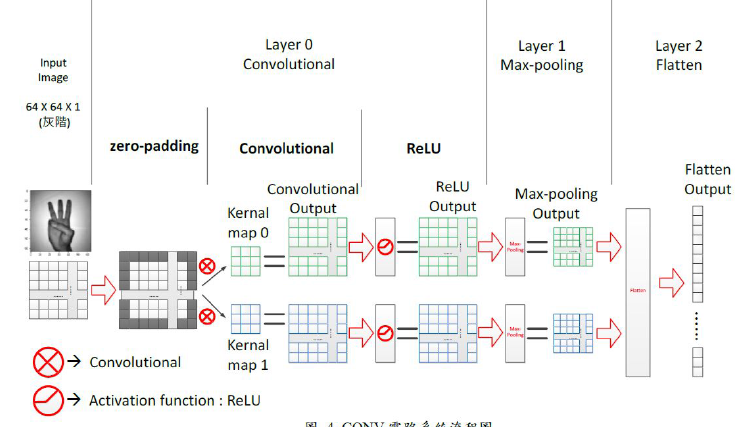


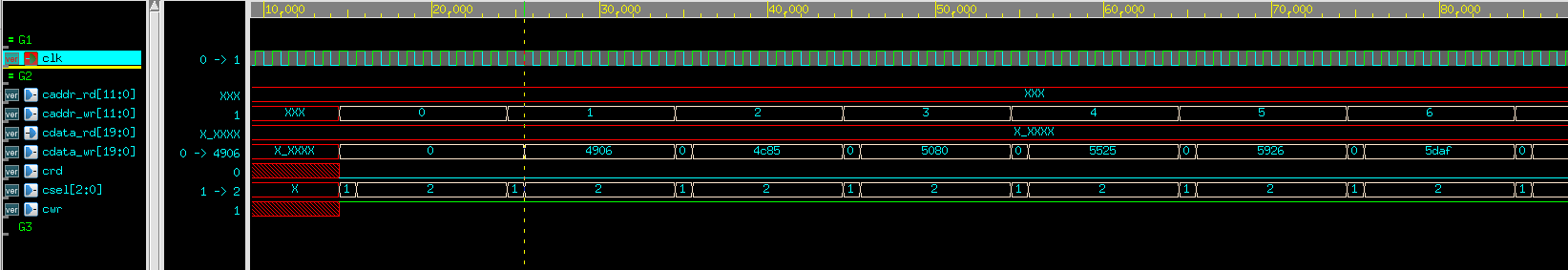
Image Convolutional Circuit include 3 main layers that is Convolution (layer 0), Max-pooling (layer 1) and Flatten (layer2).

* In the layer 0, I put in the input image and convert it into a grayscale image (the size is 64 (width) x 64 (height) pixels). After zero-padding, I use 2 kernels to convolution. The kernel is a matrix has size 3x3. Then I execute Relu operation. The result of layer 0 is two images with a size of 64x64 pixels.
* In the layer 1, I execute max-pooling operation (2x2) with stride is 2. So, the result will show 2 pictures with each of one with 32x32 pixels.
* In the layer 2, The images are flattened, we take each of width’s pixel and height’s pixel are sorted in to a sequence of 2048 (32x32x2). Beside that, Image Convolution Circuit also have memories (L0\_MEM0, L0\_MEM1, L1\_MEM0, L1\_MEM1 and L2\_MEM). The output result of each layer is stored in corresponding memory storage space.



About memory storages in Image Convolutional Circuit include:

* L0\_MEM0, L0\_MEM1, L1\_MEM0 contain output values.
* L1\_MEM1 and L2\_MEM are both RAM models with the same control method and timing. Both write and read operations are possible. Use different “csel” settings to start the output phase of each layer.
* Using “*caddr\_rd”* as the memory address and read signal data.
* About “*caddr\_rd*” will be read into “*caddr\_rd”* immediately after the trigger.
* When writing, use “*caddr\_wr”* as the memory address and “*cdata\_wr”* as the writing data signal.
* In data flow, if “*cwr”* is **High**, the data of “*cdata\_wr”* will be written to the address indicated by “*caddr\_wr*” at this time.



**Lesson learn**

(Please write down the experience of completing this assignment, what you learned, and the points of difficulty.)

After finished this homework, I learn many knowledges to design an image convolution circuit. Beside that, I can understand methods to create main function (ex: convolution, max-pooling, flatten) by Verilog.

To be honest, this homework is difficult for me. Because I recognize that the hardware language is not simple, I must imagine and draw blocks in my head when I was coding. So, I spent a lot of time to do this homework. Those are all my difficulties.